REMARKS

The Examiner stated that the information disclosure statement received on March 31, 2003 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language, for DE195 29 746. An information disclosure statement including the English version of DE195 29 746 as it was filed at the USPTO is being submitted concurrently with this response.

REMARKS

Claim Rejections - 35 U.S.C. §102

The Examiner has rejected claims 1-10 under 35 USC 102(b) as being clearly anticipated by Hieber et al. (U.S. Patent No.: 5,399,389). The Applicant respectfully traverses. Heiber does not anticipate the Applicant's claims. In particular, Heiber does not teach the elements of independent claim 1. In claim 1 the Applicant claims providing a silicon substrate, forming a trench in the silicon substrate, and forming a self-planarized dielectric layer over the silicon substrate and in the trench. In contrast, Heiber teaches forming a self-planarized dielectric layer over an aluminum interconnect that is formed on a glass substrate. Therefore, the Applicant respectfully submits that the Applicant's claim 1 and claims 2-10 that depend upon and incorporate the limitations of claim 1 are not anticipated or rendered obvious by Heiber.

Claim Rejections – 35 U.S.C. §103

The Examiner has rejected claims 16-27 under 35 USC 103(a) as being unpatentable over Hieber et al. ('389) in view of Jang et al. (U.S. Patent No. 5,786,262) and Cox (U.S. Patent No. 5,851,927). The Applicant respectfully traverses. The cited references, individually or in combination, do not teach all of the elements of the Applicant's claims. In particular the cited references do not teach the elements of independent claim 16. In claim 16 the Applicant claims a method for forming a trench isolation structure on a silicon substrate comprising applying a CVD anti-reflective coating (ARC) *on and contacting* the silicon substrate, forming a photoresist on the ARC, patterning the photoresist, etching through the CVD anti-reflective coating and through a depth of the silicon substrate to form a trench. In contrast, Heiber teaches forming a self-planarized dielectric layer over an aluminum interconnect that is formed on a glass substrate. Also, Jang does not teach forming a CVD ARC *on and contacting* a silicon substrate but rather teaches forming a silicon dioxide pad layer on the silicon substrate, a silicon nitride CMP etch stop layer on the pad layer, a thermal oxide formed on the etch stop layer, a photoresist over the thermal oxide, and then etching a trench through all of the layers. And, Cox teaches forming a gate electrode material over a silicon substrate, a dielectric nitride layer over the gate electrode material, an adhesive oxide layer over the dielectric nitride layer, a photoresist over the adhesive oxide layer, and then etching a gate stack from the layers of materials formed over the silicon substrate. Therefore, the Applicant respectfully submits that the elements claimed in Claim 16 are not taught by Heiber in view of Jang and Cox. Additionally, the claims 17 – 27 that depend upon and incorporate the limitations of claim 16 are also not taught by the combination of references. Thus, claims 16-27 are not taught or rendered obvious by the cited references either individually or in combination.

Allowable Subject Matter

The Applicant acknowledges the allowance of claim 11 and thanks the Examiner for the allowance.